

Voyetra Eight Hardware Maintenance Manual

Revision 1.0a

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1 Introduction

1.1 *Tracking Down Voices*

From time to time, this manual will refer to calibrations for a particular voice. These voices are numbered from 0-7 and are indicated on the trimmer locations diagram. However, when troubleshooting, it is often necessary to determine which voice is defective. The **Set Page** (see appendix) provides a feature for disabling voices which may be used to locate which voice is sounding.

1.2 *Is Anything Really Wrong?*

The **Voyetra** is a very complicated instrument and at times may generate sounds which may seem to indicate a malfunction when none actually exists. In case of question, the easiest way to determine if the instrument is functioning properly is to load the **Null Patch** by pressing **A440** and then pressing **Call Right** and **Call Left**. This loads the instrument with a known sound and the editing pages can be used to check for specific features.

Alternately, the Quality Control/Calibration test tape may be loaded into the instrument and the documented test procedure may be used to test all system functions for proper operation.

It is strongly suggested that a problem be verified prior to attempting any system troubleshooting.

Examples of non-existent problems are “puzzling” things like a changing timbre that doesn’t always happen. Remember that the keyboard is velocity sensitive and the timber change could very well be part of the program. Other modulation routings can cause “weird” non-existent problems such as detuning oscillators, strange tracking, etc.

1.3 *Does the instrument need a calibration?*

The **Voyetra** will rarely need calibrating since the most sensitive part of the instrument, the VCO, is automatically calibrated when **Auto Tune** is pressed. However, the VCFs, VCAs and Mod system do have calibrations that may have to be tweaked.

The following list of sample problems may help in determining what symptoms require specific calibrations:

One voice sounds “different” than the others.

First, determine what it is about the voice that is “different.” Is it the “tone?” Then it may need a VCF calibration. Is it the “level?” Then it may be a VCA calibration. Is it the “tuning?” Then it may need a Mod System calibration, or a VCO may be defective.

If the tone is different, refer to the VCF section of the manual and calibrate or troubleshoot the VCF circuits. If the level is different, refer to the MIXER section and troubleshoot the VCAs. If the Mod System is at fault, refer to the Mod System overview and then see whether it’s the ANA1, ANA2, or VCF card. If there’s a VCO problem, refer to the VCO section of this manual.

A strange “clicking” or “thumping” is heard whenever a key is pressed.

Is the click part of a patch? Play the null patch and see if it goes away. Try turning off the VCOs in the null patch to see if it’s still there. Maybe the VCA offsets on the mixer card need calibrating. Usually, only one voice is out, so you’ll have to use the SET page to find the culprit.

One program is out of tune but the rest are O.K.

This sounds like a classic Mod System “problem” where VCO modulation is on ever so slightly. A problem on “one program” is usually an indication that the program rather than the instrument is at fault.

Pitch bend on the left is different than on the right.

This may be a Mod System setting, but it can also be a calibration on ANA2 or the POT PANEL.

1.4 Card Summary

1.4.1 Mixer Card

Contains eight VCAs (one per voice) and a stereo mixer that sums the system outputs. Calibrations include CVA offset trimmers and channel gain trimmers. The MIXER also contains the Noise Source and various other minor system functions.

1.4.2 VCO Card

Contains four VCOs. The system has four of these cards, two per side.

1.4.3 VCF Card

Contains four VCFs and modulation circuitry. The system has two of these cards, one per side. Calibrations include filter scaling, initial filter cutoff and initial filter resonance for each VCF.

1.4.4 DAC Card

Contains the Voice on/off functions, and the A/D and D/A functions, which allow the CPU to control the analog system components. Calibrations include DAC offset adjustment, reference trim and mod system offset trim.

1.4.5 DIGIMOD Card

Contains system clocking logic for the modulation and DAC subsystem.

1.4.6 ANAMOD 1 Card

Contains the mod subsystem routing circuitry.

1.4.7 ANAMOD 2 Card

Contains high speed multiplexed VCAs for the mod subsystem. Calibrations include VCA offsets and gain as well as an adjustment for pitch bend LEFT and RIGHT balance.

1.4.8 CPU Card

Contains the host computer and memory circuitry for controlling the **Voyetra** and memorizing patch settings.

1.4.9 Pot Panel

Contains the Keyboard and front panel parameter trimmer interface circuits. Calibrations include pitch bend balance and gain, and X axis gains.

1.4.10 Switch Panel

Contains LEDs and switches with interfacing circuits for connecting them to the CPU.

1.4.11 Jack Bay

Contains interface jacks and an AGC circuit for the Tape input.

1.4.12 Power Supply

Contains regulators and fuses for +/- 15V, +5V, +11V, +22V, as well as power-down detection circuitry for the battery backed-up RAM on the CPU.

1.4.13 Keyboard

Contains digital and analog circuits to interface the keys and controllers to the CPU via the Pot Panel.

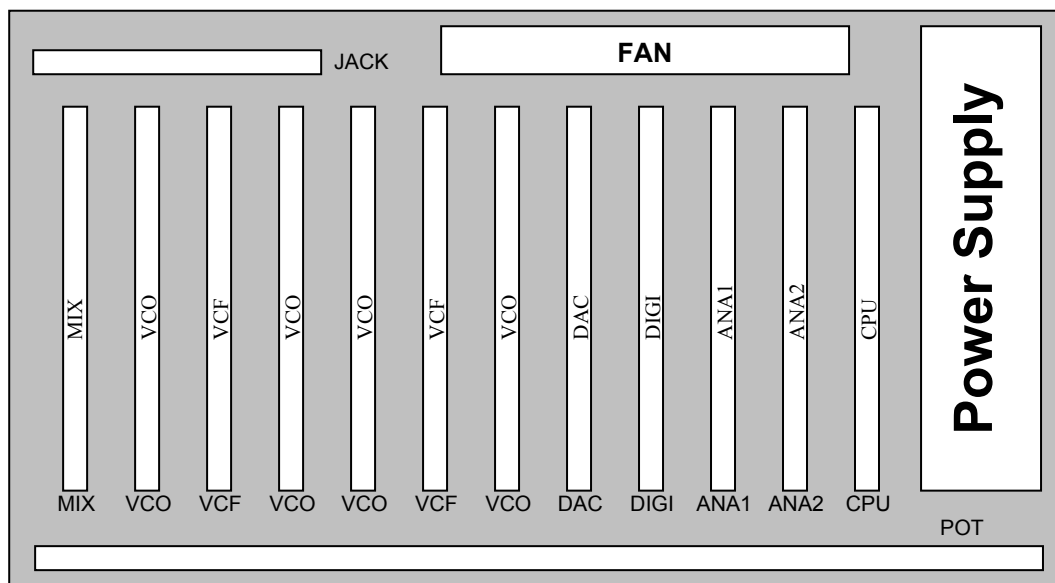


Figure 1-1 Card Placement inside the V8 Chassis

1.5 Signal Flow Diagrams

The following diagrams are included to assist in understanding some of the **Voyetra 8's** signal flow paths.

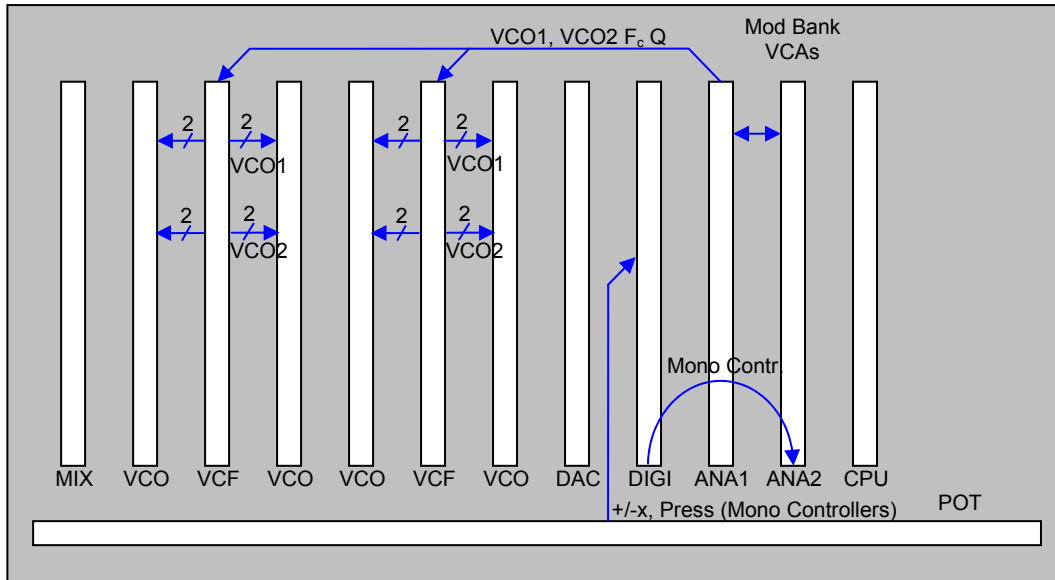


Figure 1-2 Modulation System Signal Flow

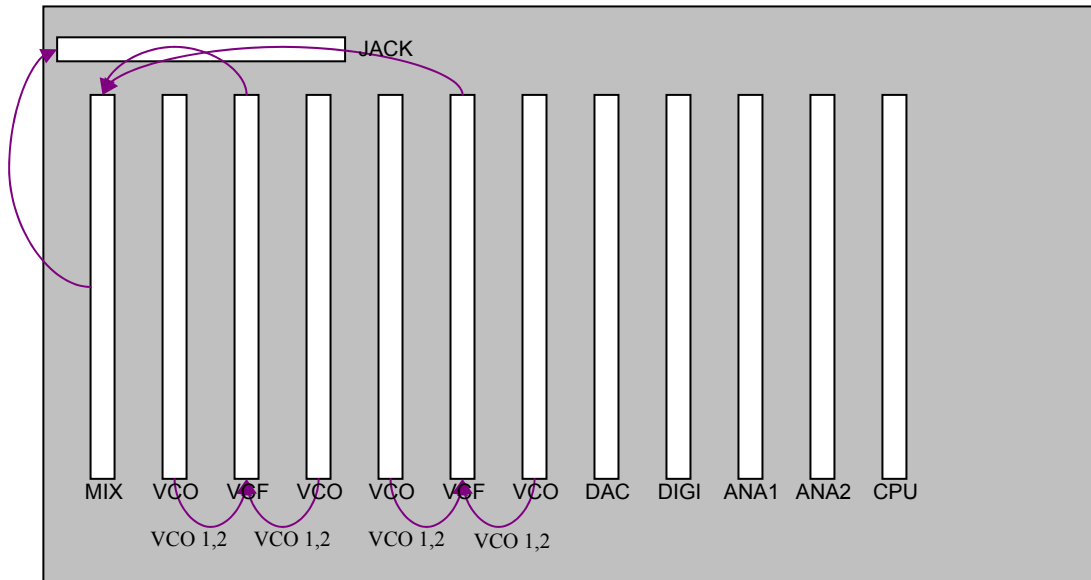
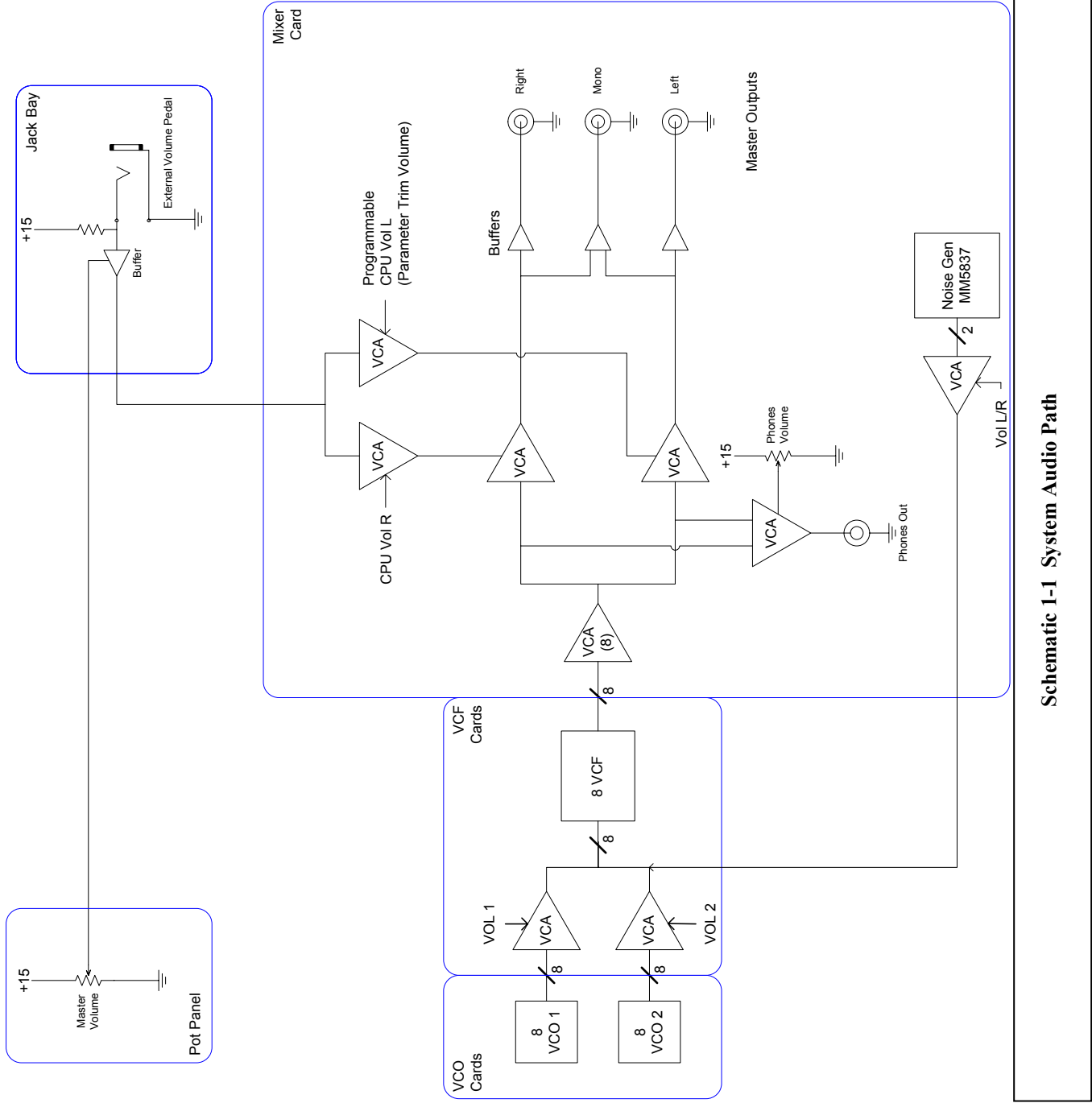


Figure 1-3 Audio Signal Flow



Schematic 1-1 System Audio Path

2 MIXER Card

2.1 Theory of Operation

The MIXER Card consists of eight identical Voltage Controlled Amplifier (VCA) circuits followed by mixing circuitry. In addition, certain other related functions are placed on this card.

The functions on this board include:

- Eight channel demultiplexer for ADSR 2 voices 0-7
- Demultiplexing for Volume L, R, Noise volume L, R, and slave synthesizer Gate, CV
- Noise generator with associated VCAs and Low Pass Filter
- Headphone Amplifier

2.2 VCA Operation

The VCAs on the MIXER Card are made up of SSM 2024 Quad VCA ICs. The audio inputs to these VCAs come from the VCF card audio outputs. Whenever a key is pressed and a voice activated, an ADSR voltage is generated at the appropriate CD4051 output and drives the VCA for that voice. This causes the VCA to pass the VCF audio at its input to the summing amp at its output. The gain is set by a trimmer in line with the ADSR signal.

The VCA outputs are mixed in four groups of two such that VCA 0 & 1 come from one op amp output, VCA 2 & 3 from another op amp output, and so on. When the keyboard WHOLE 8 Mode is selected, the output of sub-mixer 0, 1 is hard panned to one side of the VOYETRA output, while the output of sub-mixer 6, 7 is hard panned to the other side. The outputs for 2,3 and 4,5 are panned to be slightly offset from the center of the stereo spectrum. When the SPLIT or LAYER modes are selected, the outputs of 0, 1, 2, 3 are hard panned to one output while the 4, 5, 6, 7 outputs are hard panned to the other side. Of course, the MONO output always contains the sum of all eight voices.

The switching to accomplish this output panning is accomplished by using a DG308 analog switch that is turned on by a 0, +8V control signal called SPLIT/WHOLE 8 generated at the DAC CARD.

The L and R output mixers consist of two VCAs that are used to set the output level and serve as noise gates. When no keys are pressed, the CPU turns off these VCAs to quiet the system output. The output level is set by the Master Volume Control on the POT PANEL and the Parameter trimmers. The CPU digitizes the parameter trimmers and demultiplexes

them on the MIXER CARD at the points called VOLUME L, R. The Master Volume Pot is routed to the JACK BAY for processing by the external Volume Pedal, and then routed to the MIXER CARD to the point labeled MASTER VOL. These control signals are multiplied by VCAs that convert them to control currents used to derive the volume/noise gate VCAs as illustrated on the schematic.

The A440 tone comes from the DAC CARD and is turned off by the CPU. It is injected into the system audio by an inverter transistor designed to eliminate the digital noise that is present on all DAC CARD signals.

2.3 Headphones

The outputs of the VCA subchannel mixers are routed to another VCA, followed by an opamp used as a headphone driver. The front panel Headphone Volume control is used to send a control voltage to this VCA to set the headphone volume.

2.4 Noise

The noise source is generated by an MM5837 digital noise generator. This output is sent to two VCAs which set the noise L, R volume, and whose outputs are routed to the VCF cards L & R. The noise is also passed through a low pass filter whose low frequency noise output is routed to the ANAMOD 1 CARD for use as a controller in the Modulation System.

2.5 Calibrations

Any VCA will have a certain amount of DC feedthrough from its control input to the output which causes an output signal that follows the DC control signal. This sounds like a “thumping” or “clicking” when fast attack and release ADSRs are used. To compensate for this, each VCA on the MIXER CARD has an offset adjustment trimmer which must be set for minimum DC feedthrough. This includes eight voice VCAs and two for the Left Right output VCAs.

To assure that the voice volumes are all the same, individual channel volume trimmers are also adjusted.

3 VCO Card

3.1 Theory of Operation

The Voltage Controlled Oscillator Card (VCO CARD) consists of four oscillator circuits based on the CEM 3340. The system uses four identical cards, two for the LEFT side of the instrument and two for the RIGHT side of the instrument. The VCOs on the card correspond to VCO1 and VCO2 for two voices. Thus, the left and right side of the card are identical. The cards may be interchanged to facilitate troubleshooting.

The functions on this board include:

- Four VCO circuits each with Voltage Controlled Frequency, Voltage Controlled Pulse Width and Voltage Controlled Tracking.
- Waveform mixers for each oscillator
- -5V reference circuit
- VCO control voltage demultiplexers

3.2 VCO Operation

The CEM 3340 is an integrated oscillator IC that generates sawtooth, triangle and variable width pulse waves. The output of the sawtooth wave is differentiated and sent to a CD4520 divider IC to generate a square wave that is one octave below the oscillator frequency. The waveforms are summed by an LF347 wide bandwidth op amp. Since this summer is inverted, it is followed by an inverter to form positive waveform outputs that are routed to the VCF card.

The triangle and sawtooth waveforms are routed through CD4053 analog switches which are turned on or off by the DAC CARD. The pulse wave is turned off by the CPU by adjusting the control voltage that varies the pulse width to the 100% width value. This causes the pulse width to go high, which is inverted by a transistor that feeds the mixer. The sub-octave is turned off by the DAC when it toggles the rest line on the CD4520 divider.

SYNC and LINEAR FM are also turned off/on by the DAC driving a CD4053 analog switch.

Oscillator frequency is determined by the CPU tracking control voltage, CPU initial pitch control voltage, modulation input control voltage (from VCF) and pitch bend control voltage (from ANAMOD 2.) These voltages are summed directly onto the CEM3340 via 1% scaling resistors. Note that earlier model VCO cards use "blue" 1%, 100K resistor packs for this

summing network, while newer versions have this network replaced by discrete 1% 100K resistors.

3.3 ***AutoTune functionality***

When the front panel AUTOTUNE button is pressed, the CPU CARD calibrates the VCO tracking (V/Octave), initial pulse width, and initial frequency. The CPU first turns off all of the VCO waveforms except for the Sawtooth and disables the VCO pitchbend lines coming from ANAMOD 2. Then, it selects VCO1 in voice 7 (designated on the front panel displays as VCO 15) by turning on the proper slot on the VCF tuning multiplexer (see VCF CARD technical description), switching the VCO L/R switch on ANAMOD 2 (see ANAMOD 2 technical description) and selecting VCO1 on the DAC CARD (see DAC CARD technical description.) The sawtooth is then converted to a square wave by a comparator on the DAC CARD and the frequency is measured by a 68B40 timer IC on the DAC. The CPU uses this frequency to compute the correction voltage it has to send to the VCO Control Input to have it generate a frequency of 440Hz when the middle A key is pressed on the keyboard. This voltage is added to the keyboard voltage when it is sent to the VCO.

After all this, the CPU turns off the sawtooth, turns on the pulse, and uses the same system routing to measure the pulse width. It then computes the initial pulse width voltage necessary to get a 50% pulse. These measured values are stored in the Batter Backed-up RAM on the CPU (the same RAM that remembers the program settings) so that the next time AUTOTUNE is pressed, the computer knows that it can begin its calculations from the last calculations it made, even if the power is shut off.

After it finishes with VCO1 voice 7, the CPU selects VCO2 voice 7 (called VCO 14), and performs the same calculations for it. Then VCO 1 voice 6 (VCO 13) is done, etc. until all 16 VCOs (15 through 0) are calibrated.

If problems are found while the CPU is trying to tune the VCOs, a letter is displayed next to the VCO number as follows:

Letter	Problem
A	Can't sense VCO
B	?
C	?
D	?
E	Pulse wave won't turn off

Each letter corresponds to a different problem, but the only serious one is “A” since it indicates that the VCO can’t be sensed by the CPU, either because it is very low in frequency, has a DC offset on it, or is completely missing.

If you get other letters coming up, they usually go away after the second or third time you press AUTOTUNE. This is because it’s possible that the CPU didn’t get the right reading on the previous try, or that the instrument isn’t warmed up yet. Persistent letters indicate a true VCO problem.

If any letters are displayed, the CPU will disable the voice in which the defective VCO resides, so that the instrument may still be played with one less voice until it can be repaired.

3.4 DC Voltages

The card uses +/- 15V to drive the CEM 3340s and opamp ICs. The CEM 3340s also require a stable -5V reference, which is derived on board to minimize system interaction between cards. The +10V reference from the DAC is also used on this card to provide a current reference for the CEM 3340s.

3.5 Card Pin Signals

The signals coming into and out of the card are as follows:

3.5.1 Inputs

Modulation inputs for the VCOs coming from the VCF CARD
+10V reference from the DAC CARD
Power supply inputs +/- 15V and analog ground
CPU control signals for the CD4051 demultiplexers (Enables and AL0, 1, 2) coming from DIGIMOD
DAC control lines (SAW, TRI, SUB, FM, SYNC)
Pitch bend input from ANAMOD 2
Multiplexed DAC signal for 4051s

3.5.2 Outputs

VCO1 & 2 outputs for two voices

3.6 Troubleshooting Tips

These troubleshooting tips assume that the VCO test tape REV 1.0 has been loaded into the VOYETRA. If this tape is not available, the

suggestions will still prove useful if the theory section has been thoroughly understood.

3.6.1 Step 50-71: Waveform Tests

These steps check that all of the VCO waveforms are present and are of proper amplitude and frequency. Since the instrument has been AUTOTUNEd and the middle A key is down, the outputs should all be pretty close to A440. The setting of the MASTER TUNE control, the pitchbend joystick and pitchbend pedal will all affect this.

Problems with the waveforms can be traced to the CD4053 for the saw and triangle, the CD4520 for the suboctave and the pulse width control voltage coming from the CD4052 for the pulse wave.

3.6.2 Step 72-73: Sync Check

The sync function is checked here. The distinct “sync” waveform should be apparent as VCO1 is locked onto VCO2’s frequency. Problems may be caused by the CD4053 switch and the CEM3340.

3.6.3 Step 74-75: Linear FM Check

Linear FM is when the output of the VCO2 mixer is routed to the linear control current input on VCO1. Problems can be caused by the CD4053 switch or if the output of VCO2 is defective.

3.6.4 Step 76-79: Modulation Test

VCO1 and 2 modulation comes from the VCF card (see VCF technical description) and is fed into the VCOs via summing resistors on the CEM 3340s. The problem of no modulation can be caused by improper resistor values or shorts on the modulation lines.

Defective demodulation buffers on the VCF card can cause jittery oscillators if the VCF has not been checked for proper operation for the modulation demultiplexers. If jittery oscillators are found, try switching VCF cards to see if the problem follows the VCF. If so, chances are it’s in the Modulation system and not on the VCO card.

3.7 Typical Problems And Solutions

3.7.1 Letter “A” appears

This means the VCO can’t be sensed at the DAC. Check if the VCO has a sawtooth at PIN 9. If so, trace it to the waveform mixer output that

feeds the VCF card. If not, switch the CEM 3340 with a good one and see if the problem is a bad IC.

3.7.2 Letter “B,” “C” or “D” appears

This problem may not be on the VCO but instead may be coming from the VCF. First switch VCF cards to see if the letters appear on other voices. If not, then pull out the ANAMOD 1 card to make sure it's not caused by a defective modulation system. If you still have problems, chances are the problem is on the VCO card, but just to make sure, switch the bad card with a good one and see if the problem is still on the bad one. If it is, then the card is defective.

These problems can be caused by a bad CD4051, bad buffers or bad CEM3340. First switch the CD4051 with one on a voice that has no problems. If the problem now appears on the other voice, the CD4051 is bad. Then try switching the suspect CEM3340 with a known good one. If this isn't it, you'll have to try trouble-shooting the CD4051 buffer circuits and support circuitry for the CEM3340.

3.7.3 Letter “E” appears or other pulse width problems

The voltage at the CEM3340 pin 5 should be about +6V or the Pulse wave won't turn off.

3.7.4 No sub octave

Check if the input to the CD4520 has a negative spike on it. If it doesn't, then check the coupling cap and bias resistors on the input to the CD4520. If it is, check if the reset pin on the IC toggles when the suboctave is turned on and off. If it does, the CD4520 is probably bad.

4 VCF Card

4.1 Theory of Operation

The Voltage Controlled Filter Card (VCF Card) consists of four identical four-pole (-24dB/Octave) VCF circuits based on the SSM 2044 Integrated Filter. One card is used for the LEFT side of the instrument and the other for the RIGHT side of the instrument. Both cards are identical and may be interchanged to facilitate troubleshooting.

The functions on this board include:

- Four filter circuits each with Voltage Controlled Cutoff (F_c) and Resonance (Q).
- Voltage Controlled Oscillator (VCO) volume amplifiers for VCO1 and VCO2 on four voices.
- Modulation system demultiplexers for VCO1, VCO2 Filter Cutoff (F_c) and Resonance (Q).
- VCO1 and VCO2 multiplexing for the modulation/tuning system.

4.2 VCF Operation

The SSM2044 is a four-pole filter with a current input and current output. The input consists of the output currents of the VCO volume VCAs and the noise voltage dropped across the 100K noise input resistors, while the output current is converted to a voltage by the voltage-to-current converter opamp inverter TL082 U12. This output is routed to the mixer card.

The filter audio inputs include VCO1, VCO2 and Noise. The noise source is generated on the MIXER card and is routed to all four VCFs simultaneously. The VCO1 and VCO2 volume levers are determined by two SSM 2024 Quad Voltage Controlled Amplifier (VCA) ICs. The control voltage for these ICs is generated by the CPU at positions 4 and 5 on demultiplexer CD4051, U3.

VCO1 may bypass the VCF using the MC14551 quad switch to route the output current directly into the current-to-voltage converter at the output of the SSM 2044. The position of this switch is determined by the control signal on pin 6 which is generated on the DAC and controlled by the CPU. The resistive current divider at the VCO 1 output to the VCF is used to balance the relative gains of VCO1 in the normal and bypass modes.

The VCF F_c cutoff is determined by the output of the control summing amp comprised of the four opamps in the LM324 U6 and associated resistor networks. The control voltages include:

- Modulation control
 - Determined by the modulation system and demultiplexed by CD4052 U1.
- ADSR 1 control
 - Determined by the CPU and demultiplexed by CD4051 U4
 - Note that the ADSR signals are generated unconventionally with respect to the standard Demultiplexing scheme (see DIGIMOD theory)
- Initial F_c setting
 - Determined by trimmer calibration
- Keyboard Control and panel F_c setting
 - Determined by the CPU and demultiplexed by CD4051 U3

The sum of these control voltages determines the VCF cutoff while the adjustable divider network feeding pin 13 on the SSM2044 determines the filter tracking (Volts/Octave). Increases in control voltage at the summing amp input produce decreases in control voltage at the divider network since the summer is an inverting network. The trimmer labeled “V/Oct” is set so that a change of one volt at the summer input produces a one octave change in filter frequency. The control voltage is scaled down to less than +/- 100mV at the SSM2044 input pin 13 to obtain the full sweep range of 20 Hz – 20 kHz.

Filter resonance is determined by the control voltage at pin 2 on the SSM 2044, which in turn is derived from the difference amplifier LM324 U7. This difference amplifier receives a signal from the CPU (demultiplexed at CD4051 U3) that determines the initial resonance for all four VCFs on the card. The modulation signal coming from the CD4052 U1 comes from the mod system and is the result of the “Q Destination” settings in the mod banks. This signal is subtracted from the initial Q voltage and is scaled by the “Q CAL” trimmer that feeds pin 2 of the SSM 2044. Because of this subtraction, the resonance increases as the modulation signal in the mod banks decreases, thus an increasing resonance is obtained with an inverted source.

4.3 Calibrations

The VOLTS/OCTAVE trimmer is used to set the VCF keyboard tracking. When set properly, one octave change on the keyboard should closely correspond to a one octave change in F_c . The “ F_c INITIAL” trimmer is used to set all VCFs to the same cutoff for the same key down. When set properly, the VCFs should all produce an F_c of A440 when the middle A

key is pressed on the keyboard (assuming that the test programs have been loaded.) The “Q CAL” trimmer is used to set all VCFs so that they oscillate at the same resonance setting. When set properly, all of the VCFs should burst into oscillation at the same point on the front panel Q control pot.

4.4 VCO Multiplexing System

The CD4052 U19 is used to multiplex four VCO1s and four VCO2s to two independent lines called VCO1 MUX and VCO2 MUX. These signals serve two distinct purposes.

First, when the CPU is autotuning the VCOs, this multiplexer allows it to route one of the VCOs to the DAC card for frequency measurement. Secondly, it allows the modulation system to use the VCOs as modulation sources. The scanning clocks for the multiplexer, labeled VMA1 and VMA2 are derived from the CPU during autotune and from the modulation system during normal operation. This clock selection is determined by the CPU on the DIGIMOD card. The LF347 buffer amplifiers that precede the CD4052 inputs prevent the scanning clocks from leaking into the VCF audio inputs.

4.5 DC Voltages

The card uses +/- 15 Volts to drive the SSM ICs and associated audio opamps. The LM325 ICs are driven from +8V and -7V to limit their range to within the specifications of the SSM 2044 control inputs. The CD4052s used in the modulation demultiplexing are also biased with these voltages as their outputs must be bipolar while their maximum bias must be less than 16V. The F_c INITIAL trimmers are biased using a cascade transistor pair to derive a buffered reference for the trimmers as well as the -7V card voltage. The +8V is derived from a 78L08 voltage regulator driven from the +15V line.

The 15V modulation scan clocks and VCF bypass control signal are converted to 8V by the CD4050 U5 buffer to be compatible with the bias on the CD4052 demultiplexers and the MC14551 switch.

4.6 Card Pin Signals

The signals coming into and out of the card are as follows:

4.6.1 Inputs

- Modulation multiplexed inputs for F_c , Q, VCO1 and VCO2 coming from ANAMOD 1.
- Power supply inputs +/- 15V and Analog Ground

- CPU control signals for the CD4051 demultiplexers (EN 15, EN 9, AL0, AL1, AL2) coming from DIGIMOD
- Modulation scan clocks (MODEN, MA0, MA1)
- VCO multiplexer clocks (VMA0, VMA1)
- DAC control line (Bypass)
- VCO1 & VCO2 audio inputs for four voices from VCO cards
- Noise input from MIXER

4.6.2 Outputs

- VCO1 & VCO2 modulation outputs for four voices
- Four VCF audio outputs
- Multiplexed VCO1 & VCO2 outputs

4.7 VCF Card Troubleshooting Tips

These troubleshooting tips assume that the VCF test tape REV 1.0 has been loaded into the VOYETRA. If this tape is not available, the suggestions will still prove useful if the theory section has been thoroughly understood.

4.7.1 Step 00-02: Resonance (Q) Tests

These steps check that the Q control is within a specific tolerance. Problems may be caused by a defective SSM 2044, but the LM324 that derives the Q control voltage should first be suspected. Note that the four Q modulation outputs from the CD4052 U7 (and the four F_c modulation outputs) should all be at 0 V. Thus, Q calibration problems where Q will not turn off should take this into account.

In steps 00 and 01 the F_c output controls from U6 LM324 should be about 2V on pins 1, 7, 9 & 14. As in any inverting opamp circuit, the negative inputs, pins 2, 6, 9 & 13 should be at 0 V.

In step 02, pins 1, 7, 9 & 14 should have a sweeping sawtooth. Pin 13 on the SSM 2044 should have a sawtooth of about 50 mV_{pp}.

4.7.2 Step 03: DC Feedthrough Check

Ideally, the SSM 2044 should not have any output if no audio input exists. However, if the IC is defective, changes in F_c control voltage will reflect onto the output even with no audio at the input. Thus, a square wave control signal (derived from the F_c mod system) is used to check for this feedthrough. ICs which have an output square wave leakage of greater than 1 V_{pp} should be rejected and replaced.

4.7.3 Step 04-11: Initial F_c and V/Oct Calibration

These steps all check for proper F_c summing amp (LM324 U6) operation by calibrating the initial F_c setting, filter keyboard tracking (V/Oct) and

ADSR modulation depth. Problems can first be traced to the LM324 U6, but proper functioning of this IC is assured if the output follows the input. The input levels on the resistor network associated with this summing amp should be checked for conformity with a good amp. Problems with the ADSR can be traced to the output buffers/demux circuit formed by U17 (TL064) and U4 (CD4051). The buffer outputs should have a DC level of about 7V, which is the ADSR sustain level. This will vary if the ADSR mod depth is changed on EDIT PAGE 2. Again, note that the F_c modulation outputs should all be 0V.

4.7.4 Step 11-27: VCO Volume Test

These steps check for proper operation of the SSM 2024 Quad VCA ICs U22 and U23. If problems occur, first try a new IC, then check the VCO volume control voltages generated by the buffers in U15 (TL064) which should be about 7-10V when the particular VCO is supposed to be on and 0V for VCO off.

4.7.5 Step 28-31: F_c & Q Modulation

These steps check for proper operation of the F_c and Q modulation demultiplexer formed by CD4052 U1 and the associated TL068 buffers. The outputs of all the TL068s should have a sweeping LFO sawtooth if they're functioning properly. If not, check if the CD4052 inputs (pins 3 & 13) have sawtooths. If they do, check the buffers and scan the clocks on pins 6, 9 & 10 on the CD4052.

4.7.6 Step 32-35: VCO1 & 2 Modulation

This is the same as Step 28-31, except it refers to U2 and has an LFO square wave output instead of sawtooth.

4.7.7 Step 36-39: Noise Audio Path

This checks if the noise (generated on the MIXER) makes it through all four VCFs. If not, check the resistor pack inputs for noise. If it's not there, check for shorts or see if the MIXER actually has noise coming out of it.

4.7.8 Step 40-43: VCO Bypass VCF

The functioning of the MC14551 quad switch U14 is tested here. If the board passed the VCO volume tests and fails this test, then U14 is probably defective. Check, however, that the control pin 9 is actually working (this comes from the DAC) or else the switching won't occur. You can do this by switching between STEP 40 and 39 to see if the voltage pin 9 toggles between 0V and 8V.

4.7.9 Step 43: TL068 Drift Test

The TL068s serve as buffers for the modulation demultiplexers U1 and U2. If they are excessively noisy or have a high drift (which can be

determined by their offset voltage) they can cause the VCOs to jitter and sound unstable. In this step, the outputs of the TL068s are examined at a high scope sensitivity to weed out potentially bad ones. The inputs to the CD4052s are all 0V, so the TL068 outputs should be 0V as well (within +/- 5mV.)

5 DIGIMOD Card

5.1 *Theory of Operation*

The DIGIMOD Card contains miscellaneous digital and analog circuitry for modulation system and CPU card support.

The functions on this board include:

- Demultiplexing enable signals for system CD4051s
- Velocity and ADSR 2 demultiplexing/remultiplexing for the modulation system
- Mono controller mixer multiplexing
- Digital control signals for parameter trimmer addressing and other miscellaneous system functions.
- Modulation system clocks

Much of the DIGIMOD circuitry explanations refer to the description of the Modulation and DAC subsystems, and so it would be best to read those sections prior to proceeding with this section.

5.2 *Demultiplexing Enable Signals*

The DAC subsystem routes the multiplexed DAC line to 16 CD4051 demultiplexers that are located throughout the VOYETRA. The CPU must generate control signals to address these demultiplexers so that the proper analog signal may be refreshed when necessary. Since the system uses +15V to bias these CD4051s, the control signals, including address and enable, vary from 0V in logic state LOW to +15V in logic state HIGH.

When the CPU wants to route the DAC output to a particular demultiplexing location, it first selects the slot number (0-7) on the particular CD4051 by setting the low order address bits A0, A1 and A2 to the number corresponding to the position. These address bits, coming from the CPU, are +5V logic high, so they cannot be used to drive the CD4051 directly. Thus, a 7404 level shifter U5 is first used to change the levels from +5V to +15V high to form A015, A115 and A215. Then, when the CPU writes to any location in the memory mapped demultiplexers, a latch pulse is generated by the 74LS26 U4. This latch pulse is used to latch the 15V address bus by using CD4174 U14 and CD4013 U16. The outputs, now called A1015, A1115 and A1215 will not change until the CPU addresses the memory mapped demultiplexers again.

To select the specific CD4051 to be enabled, the CPU addresses one of the 16 locations on CD4515 U15, which is a 4-to-16 decoder whose outputs are normally high. When addresses, the output goes low, enabling one of the 16 CD4051s memory mapped into the system. The particular CD4051 connected to each output enable pin is labeled on U15.

Note that ENABLE 14 is split into EN14 L (left) and EN14 R (right). This is because the ADSR1 enables (EN14) are split onto VCF Card L and VCF Card R.

5.3 Modulation System Scan Clocks

The mod system scans at a rate that is totally independent of the CPU address/data lines. The clocks for this system are generated by CD4093 U17, CD4520 U9 and CD4013 U10. CD4093 is a quad Schmitt NAND gate which is used as an astable multivibrator oscillating at approximately 500 kHz. The frequency accuracy is insignificant and deviations of up to 20% are acceptable. This clock output is divided down by the synchronous counter CD4520, whose outputs are used as address clocks for the modulation system. Whenever a symbol preceded by an **M** is encountered in the VOYETRA logic description (e.g., MA0) it stands for “modulation system signal.” Thus, MA0, MA1 and MA2 are the modulation system address lines which are periodic square waves. The line labeled MODEN (MODULATION ENABLE) is a shifted enable pulse used to enable demultiplexing CD4051s in the modulation system.

5.4 Demultiplexing / Remultiplexing

The unconventional configuration of CD4051 U18 and U28 followed by CD4052 U19 and U25 are consequences of the modulation system design. The mod system uses the Velocity signals demultiplexed at the outputs of U27 and the ADSR signals demultiplexed at the outputs of U18. However, as explained in the mod system theory section, the scan rate of these signals is fixed by the modulation system. Thus, the CPU generates signals at the CD4051 outputs that look like normal individual voice signal, while the CD4052 at the outputs remultiplex the signals into two groups of four voices for the left and right sides of the system.

With this in mind, note that the address and enable lines on the CD4051s which are controlled by the CPU will be erratic, un-syncable signals while the clocks on the CD4052 (which are controlled by the modulation system clocks) are periodic stable square waves.

5.5 *Mono Controller Multiplexer*

When mono controllers are selected in the MOD BANKS, the CPU loads the respective cell in the LS670 4x4 dual port RAMs. The outputs of these RAMs are constantly scanned by the mod system and switch the controllers on or off via the CD4016 analog switch U3. This forms a “multiplexed mixer” with U1 and U2 LF356 high speed opamps. The output of this multiplexed mixer is routed to the ANAMOD 2 card for demultiplexing into eight signals that contain the summed mono controllers for banks A-D for the Left and Right sides of the modulation system.

5.6 *Miscellaneous Switching Functions*

The two CD4174 addressable latches are used by the CPU to address the POT PANEL parameter trimmers. See the POT PANEL theory for an explanation of how these trimmers are accessed. The CPU controls these latches via the level-shifted 15V address bus and data line D715.

Note that a CD4053 triple switch is used to select either the parameter trimmer addresses PA0-PA7 or the mod system scan lines MA1 & MA2. The outputs are called VMA0, VMA1 & VMA2, and are used to address the CD4052 VCO multiplexers located on both VCF Cards. When the system is tuning, the PA lines are selected to allow the CPU to control which VCO it is sensing; otherwise, the CD4052s are scanned by the mod system clocks so that the VCO outputs can be multiplexed in synchronization with the mod system scan rate.

6 Keyboard

6.1 Theory Of Operation

The keyboard receives power and clock information from the VOYETRA module. It uses this clock information to synchronize the acquisition of keyboard and analog controller signals which are multiplexed and sent to the VOYETRA module.

The functions in the keyboard include:

- Power retrieval circuits to derive +/-8 Volts from the clock/power signal sent by the VOYETRA module.
- Clock/strobe retrieval circuits to sense the sync and clock signals on the clock/power line.
- Parallel-to-serial converters to sense the positions of the 61 keys.
- Analog processing circuits for the manual controllers.
- Multiplexing/level shifting circuits to convert all of the digital and analog data into a serial data line that is transmitted to the VOYETRA module.

Before reading the circuit descriptions in this section, it would be best to review the POT PANTEL theory of operation, since much of the explanations pertaining to the operation of the keyboard data and clock/power lines is based on the POT PANEL descriptions.

6.2 Circuit Operation

6.2.1 Power Retrieval

The clock/data line from the VOYETRA module is isolated by the high speed diode D1, filtered by a 0.68 μ F tantalum capacitor and sent to 78L08 regulator U1 which generates +8V for the keyboard circuitry. The ICL7660 power inverter U2 transforms this +8V into -8V, which is further dropped to -6V via three diodes. The -6V is used to drive ICs that cannot withstand +/- 8V across their power pins (e.g., CD4051.)

6.2.2 Clock/Strobe Retrieval

The clock/power line feeds the three LM339 comparators U4 which are each biased at different levels to detect the three signals that exist on the line. The clock/power signal is divided in half by the 10K divider network so that the comparators are not driven by signals that are above their +8V supply.

The attenuated CLOCK signal transitions occur between +9V to +5V, so the top comparator is biased at about +6V to detect it. This detected signal, called CK (clock), is used to gate the shift register CD4015 U5 and the CD4021 parallel-to-serial converters U12-U27.

The attenuated DIGISTROBE signal is between +9V and +2.5V, thus the threshold for the next comparator is about +4V. The detected signal is called DSTR (digital strobe) and it is used to reset the CD4015 shift register and set the state of flip flop CD4013 U10 to the state of DIGITAL multiplexer ON, ANALOG multiplexer OFF.

The attenuated ANASTROBE is sensed by the lower comparator, whose threshold is set to about 1V. The resulting signal, ASTR (analog strobe) is used to reset flip flop U10 to the ANALOG multiplexer ON, DIGITAL multiplexer OFF mode, and reset the CD4024 analog address generator.

6.2.3 Digital Data Acquisition

When a DSTR is sensed, the flip-flop U10 turns on the CD4051 U8 and resets the serial shift register U5. The first clock pulse (CK) causes the shift register U5 to advance its D input (pin 15) to its first output, Q0 pin 13. This Q0 high state is inverted by one of the dates in CD4011 U6 and latches all of the edge-triggered CD4021s connected to the LATCH UB (latch upper bus) line when the gate transition from low to high occurs.

Since state Q1 on the CD4015 is still low, the LOEWR BUS BAR is in the LOW state while the UPPER BUS BAR is in the HIGH state as a consequence of the CD4049 inverter U7 which buffers the Q1 pin. Thus, all keys that are not down, *i.e.* on the UPPER BUS BAR, will be latched as a HIGH state on the LATCH UB CD4021s.

When the next clock pulse (CK) occurs, the CD4015 advances one more state so that Q0 and Q1 are now both high. Thus, the UPPER BUS is now LOW while the LOWER BUS is now high. When the next clock comes along, CD4015 Q2 output goes high and on this transition, the LATCH LB CD4021s are loaded with the state of the contacts, which if they're down, *i.e.* on the LOWER BUS BAR, will be latched as a HIGH state on the LATCH LB CD4021s.

At this point, all of the UPPER BUS CD4021s have HIGH logic states at the points where keys were not pressed, all of the LOWER BUS CD4021s have HIGH logic states where all keys were fully pressed, and those positions where neither slot is high correspond to keys in transition.

When the next clock comes along, the CD4015 advances a HIGH to the Q3 output, which gates the CK line onto the CD4021 clock inputs. This enables the CK line to shift out the data that was loaded during the first

three clock pulses. Thus, whenever the VOYETRA module wants to see the state of a key, it sends a clock pulse and the next cell is advanced.

The output of the CD4021s is routed to the CD4051 U8 address pins, while the inputs to the CD4051 are three voltage levels: +8V, -6V and ground. When the outputs from the CD4021s are both LOW, input 0 (or ground) is selected. This corresponds to a key in transition. When the outputs are LOW and HIGH, or CD4051 position 1, the +8V is selected, signifying a key up. When the outputs are HIGH and LOW, the -6V is selected, signifying a key down. In this way, the three possible key positions that are encoded by two binary digits are converted to a tri-level signal that can be sent on one line.

6.2.4 Analog Data Acquisition

When the VOYETRA module is through sensing all of the key positions, it sends an ANALOG STROBE down the clock/power line. This is sensed as ASTR and resets the CD4015 so all of the outputs are again LOW, disabling the CD4021s. The CD4013 flip-flop now changes state to disable the digital level translator (CD4051 U8) and enables the analog multiplexer (CD4051 U9). The ASTR also sets the outputs of the CD4024 divider to a low state, addressing the first input of U9, which is the +/- Y line.

When the VOYETRA module wants to process the next analog controller, which in this case is the +/- X line, it sends a clock pulse which is sensed as CK and sent to the CD4024 clock input to advance the CD4051 to the next position. Then another clock is sent to advance it to the pressure position. The last five positions are not used, and are meant for future expansion.

The outputs of U8 and U9 are tied together and buffered by opamp U3 which is configured as a line driver. This data output is sensed by the module as keyboard data and processed by the POT PANEL.

6.2.5 Keyboard Pressure Sensor

The keyboard pressure is sensed by two reflective sensors on either side of the keyboard frame. As the keyboard is pressed, the frame moves closer to the sensors, thus increasing the amount of reflected light. This is converted to a voltage and processed by the LM324 opamps that allow gain and offset to be calibrated. The user adjustment on the pressure allows the threshold to be set so that the onset of pressure may be adjusted.

6.2.6 Joystick

The joystick is biased by +8V and the X & Y potentiometers are processed by identical opamp level shifters that are used to set zero volts out for vertical joystick position. The outputs of these circuits are followed by balance trimmers to adjust the gain in both directions.

6.3 Calibrations

Pressure calibrations include offset for left and right pressure sensors, gain adjustment for left and right pressure sensors, gain adjustment for left and right pressure sensors and balance.

Joystick calibrations include offset adjustment for X and Y axes and +/- gain balance for X and Y axes.

6.4 Keyboard Troubleshooting Tips

It is important to realize that in normal operation, the clock/power line and keyboard data line are scanned at a rate that is determined by the CPU in the VOYETRA module. As such, it will be virtually impossible to sync on these signals with a conventional oscilloscope since they are not periodic.

7 Pot Panel

7.1 *Theory of Operation*

The Pot Panel serves two major functions:

Keyboard Interfacing. The VPK-5 keyboard clock/power signal is generated under control of the CPU. The keyboard digital data is detected and sent to the CPU. The keyboard analog data is demultiplexed and routed to the DIGIMOD card.

Parameter Trimmer Interfacing. The Parameter Trimmers are multiplexed and routed to the DAC card for digitizing.

7.2 *Keyboard Clock/Power Interface*

The CPU card controls the keyboard by sending commands on the power line that drive the keyboard circuitry (see KEYBOARD THEORY section.) The 74LS138 U1 is controlled by the CPU via the address bus selection of one of eight outputs. These functions are:

- Demultiplexer Enable (DEMUXEN): The CPU uses this line to turn on the CD4051 system demultiplexers. When a CD4051 is to be written to, the CPU writes to the 74LS138 position 3, which sets flip-flop 74LS279 LOW. When done, the CPU writes to location 4 and sets the flip-flop HIGH. This DEMUXEN line drives a 16 channel demultiplexer on DIGIMOD that drives all of the system CD4051s. In normal operation, the DEMUXEN line should always be active, *i.e.* pulses should always be present since the CPU will always be refreshing the system CD4051s.
- Clock (CLK): The Keyboard needs a clock signal to shift the digital data through the parallel-to-serial converters that are connected to the contacts (see Keyboard Theory of Operation.) When the CPU wants to access this data, it writes to the 74LS138 position 0.
- Digital Strobe (DSTR): When the CPU needs digital data from the keyboard, it generates a strobe pulse to set the keyboard logic to digital access mode. This is done by writing to 74LS138 position 1.
- Analog Strobe (ASTR): When the CPU needs analog keyboard data, it generates this strobe and toggles the keyboard logic to analog mode. This is done by writing to 74LS138 position 2. When in analog access mode, the circuitry that follows the 74LS138 automatically generates a slower analog clock.

- Analog Clock Off (ACKOFF): When the CPU is done receiving analog data, it turns off the analog clock by writing to 74LS138 position 7.

Note that in normal operation, all of these outputs should be active so that a Logic Probe connected to any of these lines will flash to indicate the presence of pulses.

The signals generated by the 74LS138 are too narrow to be used for keyboard control. As such, they are stretched by the LS279 flip-flops coupled to the LS165 shift register. These stretched pulses are called CKA, DSTRA and ASTRA and drive the LS138 U24 demultiplexer which guarantees that the three strobes will not overlap when driving the level shifter/power circuit that drives the keyboard. The LS138 outputs 0, 2, 4 & 5 are combined by the 7407 and associated transistors to generate a tri-level clock/data signal.

The power for this section is supplied by two voltage regulators to provide +18V for the signal peak, +10V for the clock level, +5 for the DSTRA and Ground for the ASTRA. The voltage regulators are driven by the unregulated +21V supply, which is fused on the power supply board.

In normal operation, the clock/power line should always be active. Since the CPU demands information from the keyboard whenever it deems it necessary, it will be virtually impossible to sync onto this signal; however, it should be possible to see the three distinct voltage levels on a good quality oscilloscope.

7.3 Keyboard Data Interface

The data coming from the keyboard is both analog and digital. The analog data corresponds to the controllers for joystick X and Y as well as keyboard pressure. The digital data corresponds to key position.

7.3.1 Digital Data Retrieval

The digital keyboard data corresponds to 61 keys and one switch (Fwd/Rev). Each key (and the switch) may be either up, down or in transition, corresponding to data voltage levels of + voltage, - voltage or zero voltage respectively. The opamp buffer LF356 U13 buffers the keyboard data for processing by the analog demultiplexers and comparators.

LM311 U11 and U12 are used to detect the key up and key down transitions. The outputs of these LM311s are connected to the CPU data bus bit D7 using the LS125 tri-state gates U9. Selection of the key up

and key down information is determined by the Chip Select (CS) lines CS UB (for Upper Bus, or Key Up) and CS LB (for Lower Bus, or Key Down). Again, since the CPU will always be accessing the keyboard, these lines should always be active.

7.3.2 Analog Data Retrieval

The buffered keyboard data is also routed to the analog demultiplexing circuitry comprised of CD4051 U14, CD4024 U8 and CD4051 U7 with associated subcircuits. The CD4024 is clocked by the same circuitry that generates the keyboard analog clock and uses the CD4051 U7 to generate an ENable pulse to drive the CD4051 U14 synchronously with the keyboard analog data that is being received. This analog data, which may have both positive and negative transitions, is demultiplexed and buffered at the U14 outputs and processed for use in the analog portions of the VOYETRA. Since the CPU will always be scanning the keyboard analog data, the control signals on these ICs should always be active in normal operation.

7.3.3 Controllers

The Pitch Bend (Joystick Y axis), +/- X joystick and pressure controllers that are demultiplexed by U14 are further processed by the analog circuitry that follows the LM324 U16 buffers. The CD4053 switches allow the VOYETRA to be controlled by a slave when they are switched to the “external” positions. This is set by the CTRL KBD line that comes from DIGIMOD. Also, Pitch Bend for the Left and Right sides of the VOYETRA can be turned off with the CD4053 switches that precede the U17 inverters. The pressure controller is buffered and sent to DIGIMOD. The +/- X controller is split into +X and -X, then sent to DIGIMOD.

7.4 *Parameter Trimmer Multiplexer*

The CD4051s U20 and U21 are used to multiplex the front panel potentiometers. The CPU selects the pots by controlling the CD4051 positions via the Pot Data (PD) lines PD0, PD1, PD2 and PD3 that are generated on DIGIMOD. The multiplexed pot information (PANALOG) is routed to the DAC card and digitized for use by the CPU. Since the CPU constantly scans the pots in normal operation, the PANALOG and PD lines should be dynamic signals.

7.5 *Master Volume and Master Tune Controls*

The Volume Control has no active circuitry associated with it. The pot derives its voltage and ground from the jack bay where it is processed and routed to the MIXER card. The Master Tune pot is routed to the pitch bend buffers and is used to transpose the entire instrument uniformly.

7.6 Calibrations

The calibrations on the pot panel are associated with the pitch bend and X controller. The pitch bend that is received from the keyboard must be adjusted so that the up and down range is consistent between VOYETRA modules. Thus, the trimmer/diode network that follows the pitch bend buffer allows balance to be set, while the gain controls for pitch bend left and right adjust for pitch bend range uniformity in both left and right halves of the instrument.

The +X and -X controllers are also trimmed to provide consistent ranges between instruments.

Consult the QUALITY CONTROL section of this manual for calibration procedures pertaining to the pot panel.